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Enhancing Power Supply Rejection Ratio for Low-Jitter Clocks

Today's electronic systems require advanced design from top to bottom. Cost and performance optimization is important in all applications, and power delivery and noise coupling concerns are as critical as ever. With jitter budgets tightening, advanced mixed-signal clocking ICs are on the front line of these design issues. Let's examine the primary sources of power supply noise, why some timing circuits are sensitive to power supply noise and how to minimize the impact of noise in jitter-sensitive applications.

Power Supply Noise Induces Jitter

Timing signals rely on accurate clock edges. When the clock edge deviates from its ideal position in time, the deviation is called jitter. Each application has a maximum amount of tolerable jitter, but the higher the clock rate, the lower and tighter the jitter requirement becomes. High-speed applications, such as Optical Transport Networking (OTN), 10 Gigabit Ethernet, Fibre Channel and 3G HD SDI have clock periods as low as 100 picoseconds. Some of these applications can only tolerate 10 to 20 picoseconds of total clock jitter before it starts impacting system performance and bit error rate. Poorly designed clock and oscillator ICs that do not implement power supply noise rejection on chip can easily couple and amplify noise, producing tens of picoseconds of clock jitter and undermining system performance. At that point, the system designer has no choice but to track down the source of the noise and minimize its impact. This extra effort increases design time, component cost and complexity of the power delivery design.

Sources of Noise

If power supply noise is a key concern in a design, there are multiple sources to investigate. One is the ripple induced by switching power supplies. Switching power supplies operate by transferring energy from the source to the load through an inductor. Constant charging and discharging at rates between 100 kHz and 1 MHz induces ripple that approximates a saw-tooth waveform.

The magnitude of the ripple depends on several factors. For example, reducing the equivalent series resistance (ESR) of the load capacitors decreases the parasitic I-R drop of the capacitors and reduces its contribution to the ripple. Increasing the switching frequency may also help since the period between charge and discharge can be reduced. More elaborate techniques include multi-phase control that further reduces the period between charge and discharge. Any of these techniques may be implemented but can result in cost, board space and design complexity penalties. In practice, minimizing output ripple below 20 mVp-p is a major challenge, especially in high-power systems. Ripple as high as 100 mVp-p is common in some networking and computing applications.

Power supply noise can also be induced by neighboring ICs. As large digital and analog devices power on and off, drive heavy output loads or switch wide output banks, they induce perturbations on the power rail that ripple through the power plane and couple into neighboring subsystems and ICs. For example, simultaneous switching noise in large FPGAs where hundreds of output buffers are driving heavy capacitive loads is a common challenge.

If simultaneous switching is a concern, using differential output buffers on large I/O banks, increasing power supply decoupling, and careful power plane design with good isolation between ICs are all essential techniques. Each of these practices can help reduce this type of noise, but cost, feature and design constraints may prevent the designer from using any of these techniques.

Ironically, systems that require the best jitter performance tend to contain the greatest amount of power supply noise. It's best to select components that provide immunity to this type of noise across a wide spectrum.

Impact of Power Supply Noise in Timing Devices

Although power supply noise can be mitigated, attenuating it to zero is practically impossible. Knowing the impact that noise has on the system is critical to determining the level of design devoted to reducing power supply noise. For clocking circuits, power supply noise translates into additional jitter, which can occur through several mechanisms.

Traditional XOs are very simple circuits that include an inverting amplifier driving a crystal. Because low-jitter XOs are so simple, vendors often overlook the need for power supply noise rejection. In many cases, the amplifier is designed, tested and evaluated only in low-noise environments. Being primarily an analog circuit, sensitive nodes can easily couple noise. That noise will translate to output jitter in the form of spurs that modulate the fundamental oscillation frequency. The more sensitive the amplifier, the higher the spur magnitude will be for a given amount of noise.

VCXOs present another problem. Typically, a varactor placed in parallel with the crystal is used to pull the crystal frequency. The varactor introduces a capacitive coupling path from the power rail directly to the oscillator input. Being the point of highest gain, even the slightest coupling can impact jitter.

Another fundamental timing circuit is the phase locked loop (PLL). PLLs are important because they are used to multiply frequencies, clean jitter or synchronize systems. The traditional analog PLL comprises of a phase detector, loop filter, VCO, output driver and feedback divider. The PLL is a feedback system that requires high-gain circuits. For example, the VCO gain is typically very high to provide a wide capture range and guarantee lock across all conditions. Inevitably, this increases the sensitivity to external noise. In many cases, a small amount of power supply ripple can couple into the most sensitive nodes and be amplified to induce very high jitter on the output. Depending on the architecture, the loop filter may also be a point of sensitivity.

Power supply noise is dominated by deterministic signals that show up as spurs on the output of timing ICs and the line output of the system. Using a spectrum analyzer is a good way to detect VDD noise. For example, if the power supply is switching at 300 kHz and the XO output is 156.25 MHz, it will be possible to observe spurs at 156.55 MHz and 155.95 MHz with additional lower magnitude spurs at 300 kHz intervals.

Novel Solutions for Noise Reduction

Although there are system solutions to power supply noise, the best remedy is to use timing components that reject external noise. Novel timing devices use cutting edge-techniques to provide ultra-low jitter that is minimally affected by power supply noise.

For example, Silicon Labs' DSPLL[®] technology, based on a patented digital control algorithm, enables all the functionality that traditional analog PLLs provide but with precise digital control. Using digital circuitry that includes a digital low-noise variable oscillator instead of an analog VCO reduces sensitivity to analog influences. Furthermore, on-chip, low-noise regulators enhance isolation from power rail noise. The result is a low-jitter technology that can be used in very noisy environments.

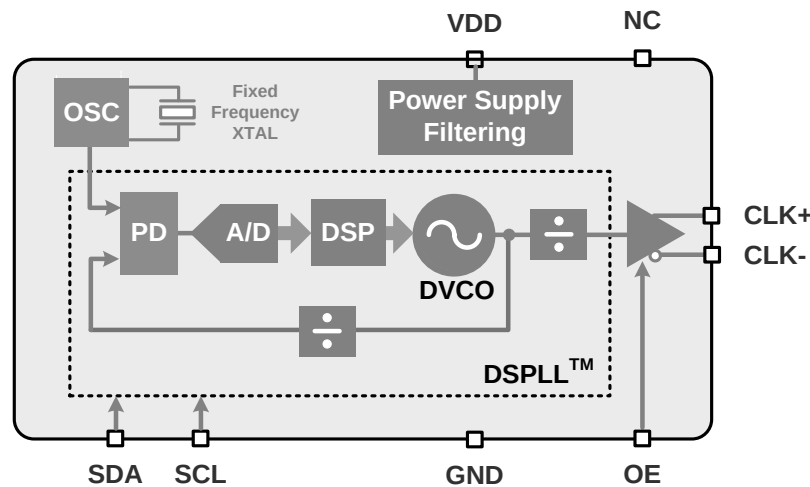


Figure 1. Silicon Labs DSPLL-Based Programmable XO with On-Chip Power Supply Regulation and Filtering

A simple comparison between a DSPLL-based XO and traditional XO technology shows the advantage of using all digital techniques and on-chip power regulation in low-jitter timing devices. Figure 2 shows the increase in output clock jitter when 100 mVp-p sinusoidal noise is injected into the XO power supply. Sweeping the noise from 100 kHz to 10 MHz and measuring the additive RMS jitter shows that switching noise can significantly degrade the jitter performance of even the highest performance XOs that do not have on-chip power regulation and power supply filtering. In contrast, DSPLL-based timing devices maintain consistently low jitter operation, even in the presence of significant board-level noise.

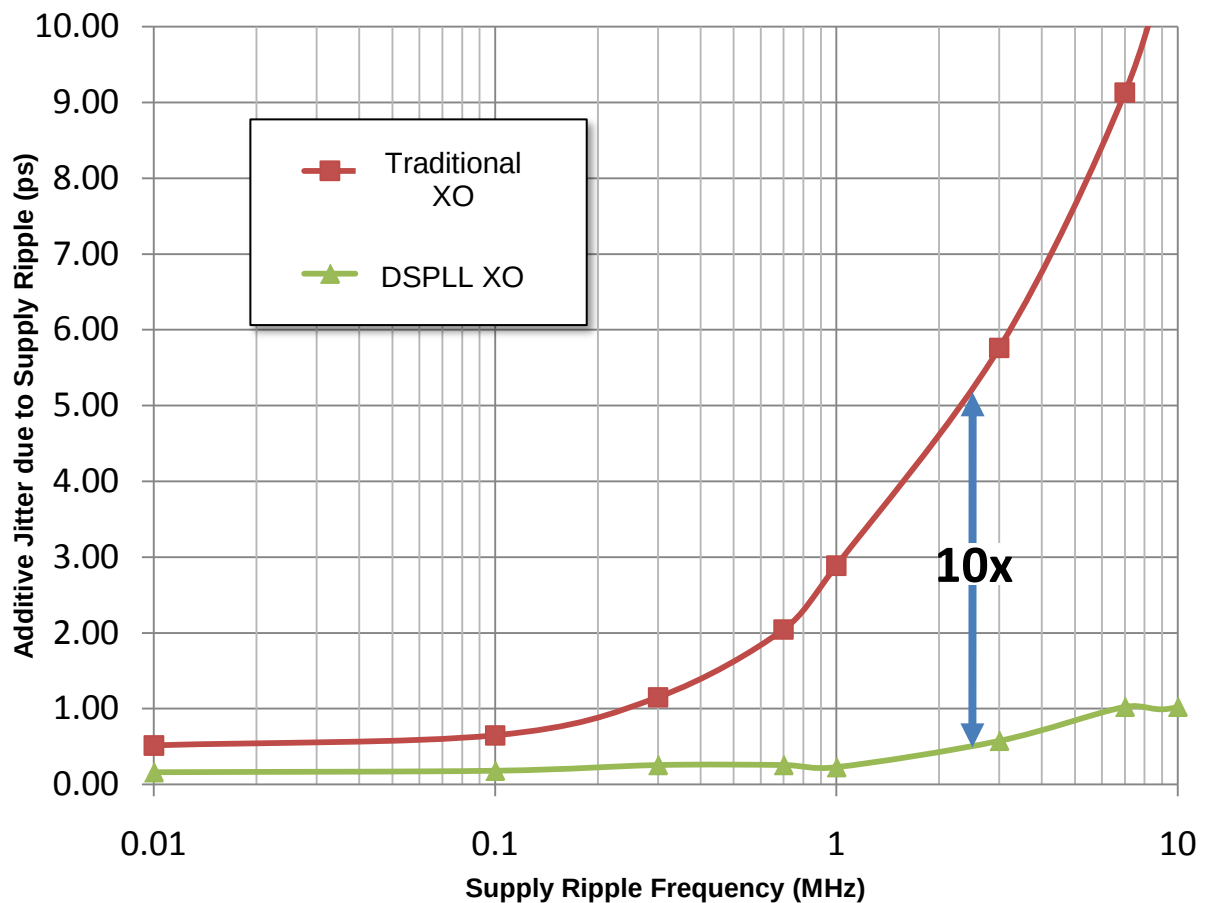


Figure 2. Additive Jitter of Traditional XOs is 3x to 10x Greater than DSPLL-Based XOs

Conclusion

In jitter-sensitive applications, power supply noise sensitivities increase design complexity and reduce functional design margin. Using advanced technology that is highly immune to external noise is an effective way to mitigate design problems before they occur. End system designers can rely on DSPLL-based XOs, VCXOs and clock devices to achieve 10x better power supply rejection ratio (PSRR) performance over equivalent traditional XOs, even in noisy conditions. This approach saves design time, minimizes complexity and reduces the need for excessive power supply decoupling.